CLAIMS

What is claimed is:

1. A circuit coupled to an integrated circuit on a die that includes:

a pulse manipulating circuit to selectively manipulate at least one pulse in a clocking signal, the manipulate including at least one of increasing the frequency of a leading edge, decreasing the frequency of a leading edge, increasing the frequency of a trailing edge, decreasing the frequency of a trailing edge, and manipulating a voltage of the at least one pulse; and

an identification circuit coupled to the pulse manipulating circuit to automatically identify an at least one pulse in each of a sequence of clock signals and to transmit the identified at least one pulse to the pulse manipulating circuit wherein the pulse manipulating circuit is to manipulate a frequency of each identified pulse in each clocking signal in response to the transmitted identified at least one pulse in each clock signals.

2. The circuit defined in claim 1 wherein the identify is based on an algorithm.

3. The circuit defined in claim 1 that further includes:

a clock signal generating circuit to generate each of the clocking signal, that is coupled to the pulse manipulating circuit

4. The identification circuit defined in claim 1 that is further to determine whether to terminate the identification based on a terminating condition.

5. The circuit defined in claim 1 wherein the identify is based on a data to be transmitted to the identification circuit from a terminal of the integrated circuit.

6. The identification circuit defined in claim 1 wherein the identify is based on an algorithm that includes one of incrementing the pulse identification up in sequential clocking signals, and decrementing the pulse identification down in sequential clocking signals.

7. A method of inputting a clocking signal to an integrated circuit comprising:

(a) a clock manipulating circuit on a die receiving a clocking signal;

(b) the clock manipulating circuit manipulating an identified pulse of the clocking signal received in (a) and transmitting the clocking signal with the manipulated identified pulse to the integrated circuit;

(c) a clock manipulation identifier circuit on a die automatically identifying a pulse to manipulate for a next clocking signal;

(d) sending a next clocking signal to the clock manipulating circuit;

(e) the clock manipulating circuit sending the pulse identified in (c) to the clock manipulating circuit;

(f) the clock manipulating circuit receiving the pulse sent in (e); and

(g) the clock manipulating circuit manipulating the pulse received in (f) in the next clocking signal sent in (d), and transmitting the clocking signal with the manipulated identified pulse to the integrated circuit.

8. The method defined in claim 7 further including determining whether the next clock meets a target terminating condition and if it does not, repeating (c), (d), (e), (f), and (g).

9. The method defined in claim 8 wherein the determining is based on a data transmitted to a terminal of the die.

10. The method defined in claim 7 wherein the manipulating the pulse and the manipulating an identified pulse includes at least one of increasing a frequency of a leading edge, decreasing a frequency of a leading edge, increasing a frequency of a trailing edge, a decreasing a frequency of a trailing edge, and manipulating a voltage of the pulse.

11. The method defined in claim 7 wherein the clock manipulation identifier circuit identifying a pulse depends upon one of a predetermined basis and received basis.

12. The method defined in claim 11 wherein the received basis includes an identified pulse transmitted to a terminal of the die.

13. The method defined in claim 7 wherein the clock manipulation identifier circuit identifying a pulse is determined by an algorithm.

14. An integrated circuit that includes:

pulse transforming means for transforming at least one pulse in each of a plural number of received clocking signals, the transforming including at least one of increasing the

frequency of a leading edge, decreasing a frequency of a leading edge, increasing a frequency of a trailing edge, decreasing a frequency of a trailing edge, and transforming at least one voltage of the pulse; and

identification means for automatically identifying an at least one pulse in each of the plural number of clocking signals, and for transmitting the identified at least one pulse to the pulse transforming means.

15. The integrated circuit defined in claim 14 that further includes clock generating means to generate each of the clocking signal, that is coupled to the pulse transforming means.

16. The identification means defined in claim 14 that is further for determining whether to terminate the identification based on a terminating condition.

17. The identification means defined in claim 16 wherein the terminating condition is to be transmitted to a terminal of the integrated circuit.

18. The identification means defined in claim 14 wherein the identifying is based on an algorithm.

19. The identification means defined in claim 18 wherein the algorithm includes at least one of incrementing the identified pulse in each successive clock signal and decrementing the identified pulse in each successive clock signal.

20. The identification means defined in claim 14 further for determining whether to terminate the identifying based on a terminating condition.

21. The identifying means defined in claim 20 wherein the condition is based on data to be transmitted to the identifying means from a terminal of the integrated circuit.

22. An integrated circuit that includes:

a pulse transforming circuit to transform at least one pulse in each of a plural number of received signals, the transform including at least one of increasing the frequency of a leading edge, decreasing a frequency of a leading edge, increasing a frequency of a trailing edge, decreasing a frequency of a trailing edge, and transforming at least one voltage of the pulse; and

an identification circuit to automatically identify an at least one pulse in each of the plural number of signals, and for transmitting the identified at least one pulse to the pulse transforming circuit.

23. The integrated circuit defined in claim 22 that further includes a clock generating circuit to generate each of the clocking signal, that is coupled to the pulse transforming circuit.

24. The identification circuit defined in claim 22 that is further to determine whether to terminate the identification based on a terminating condition.

25. The identification circuit defined in claim 24 wherein the terminating condition is to be transmitted to a terminal of the integrated circuit.

26. The identification circuit defined in claim 22 wherein the identify is based on an algorithm.

27. The identification circuit defined in claim 26 wherein the algorithm includes at least one of incrementing the identified pulse in each successive clock signal and decrementing the identified pulse in each successive signal.

28. The identification circuit defined in claim 22 further to determine whether to terminate the identifying based on a terminating condition.

29. The identifying circuit defined in claim 28 wherein the condition is based on data to be transmitted to the identifying circuit from a terminal of the integrated.

30. The integrated circuit defined in claim 22 wherein the received signals include clocking signals.